



FIG. 2

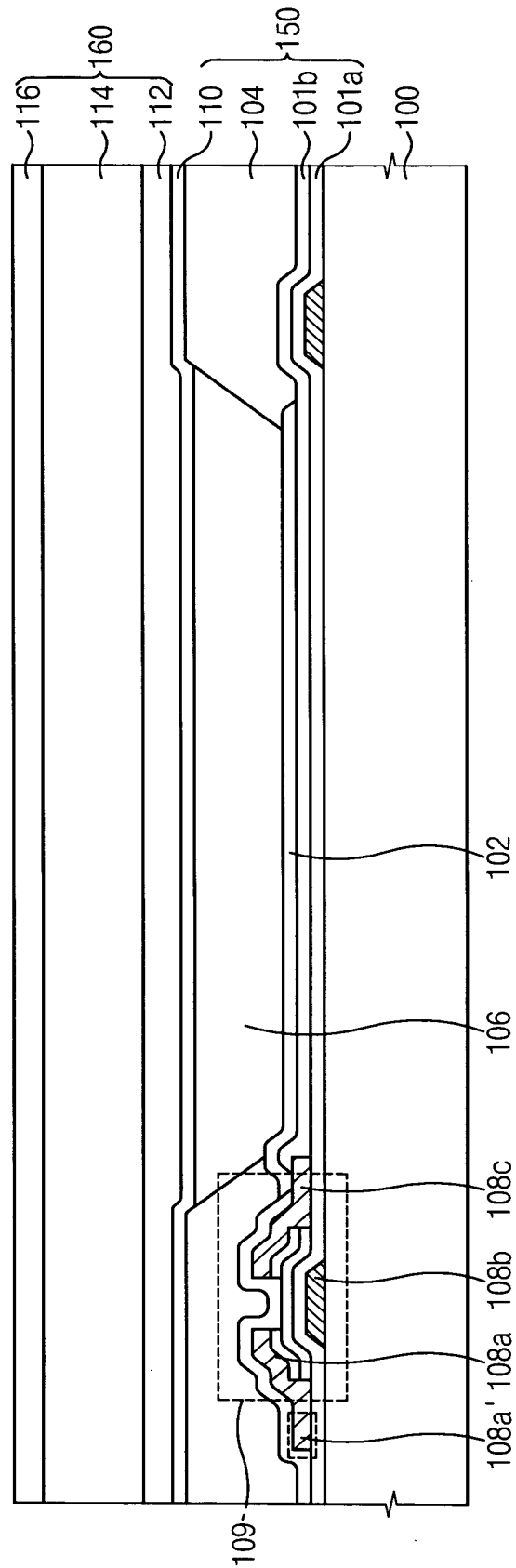


FIG. 3

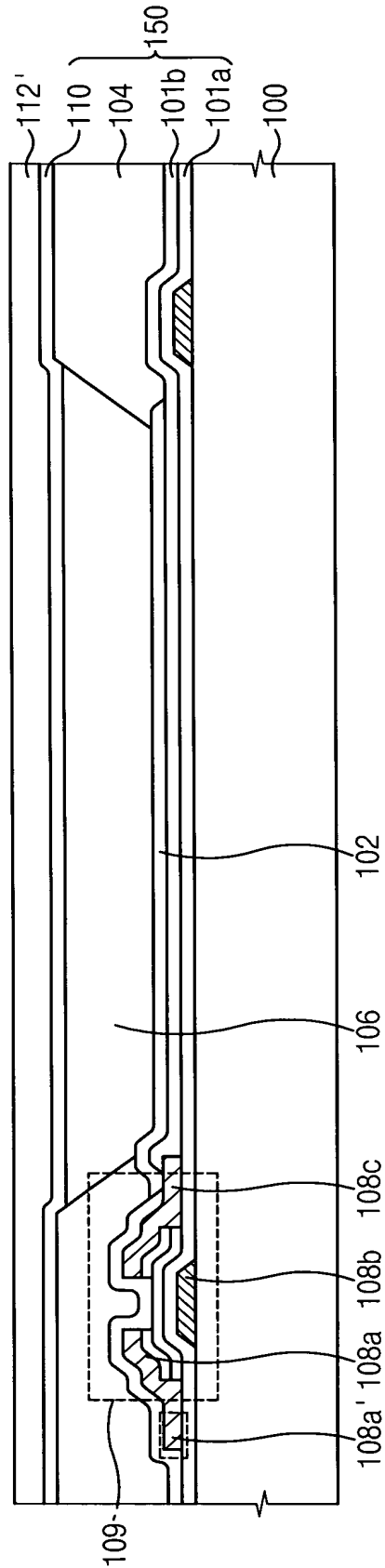


FIG. 4

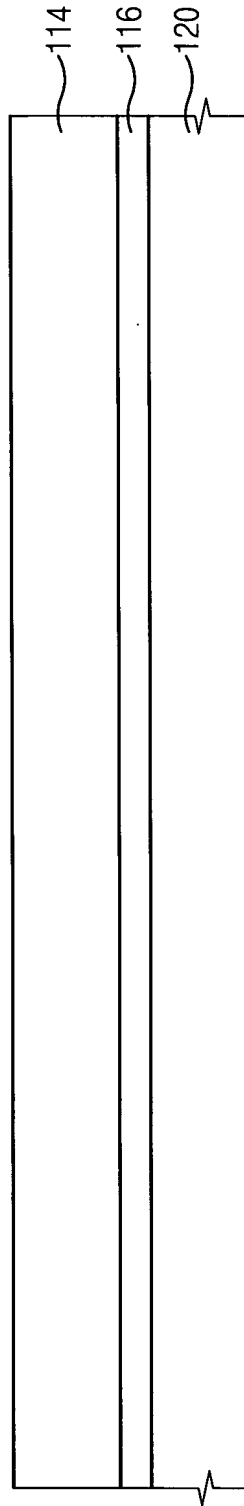


FIG. 5

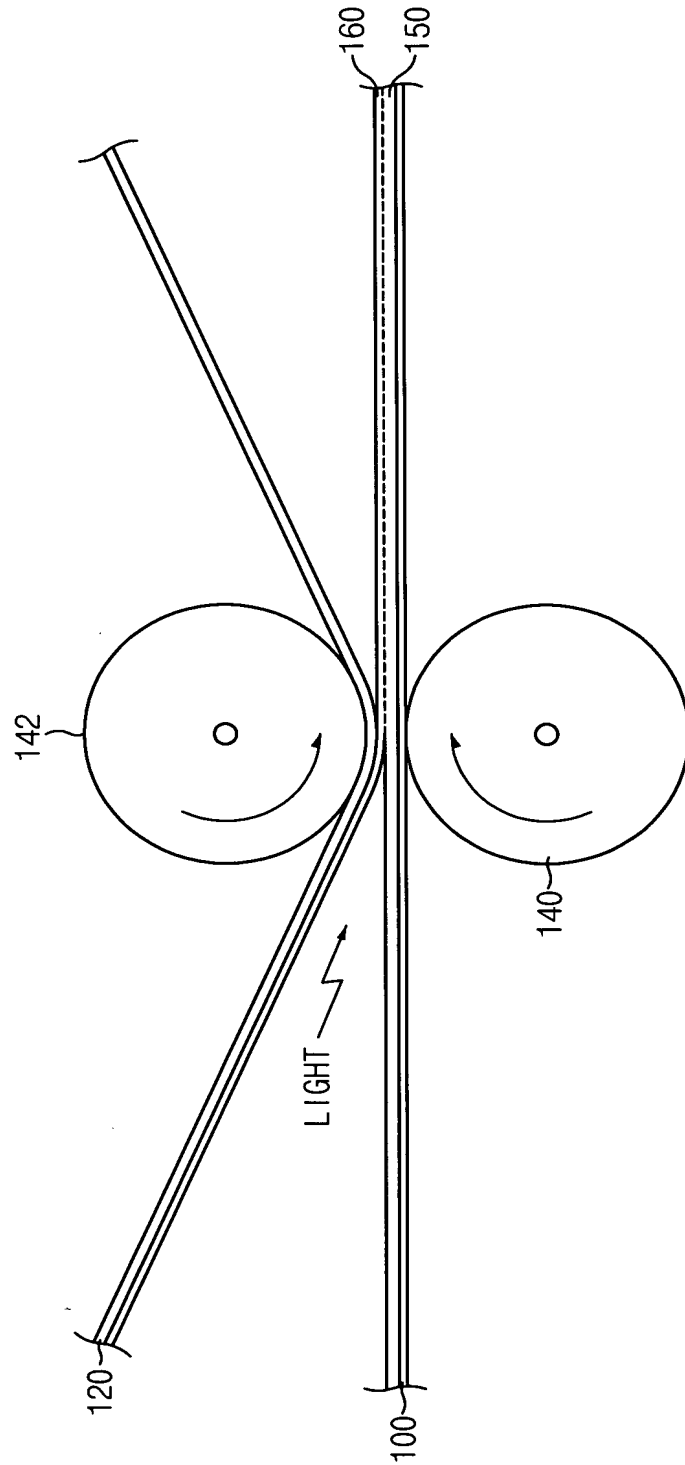


FIG. 6

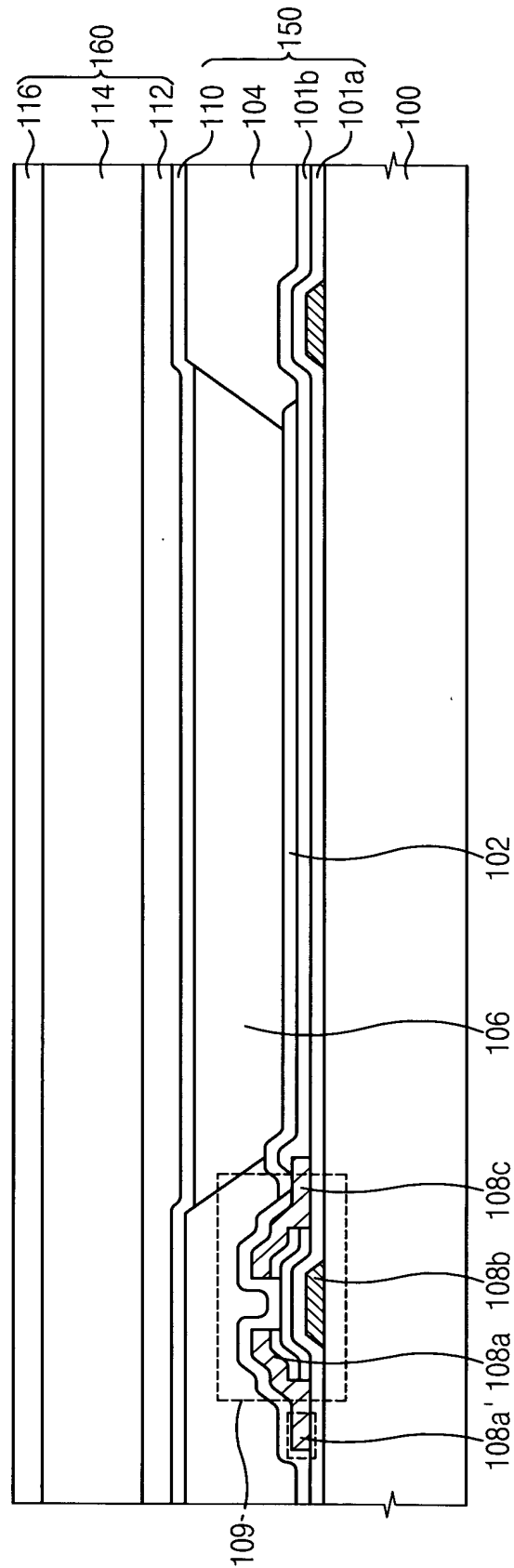


FIG. 7

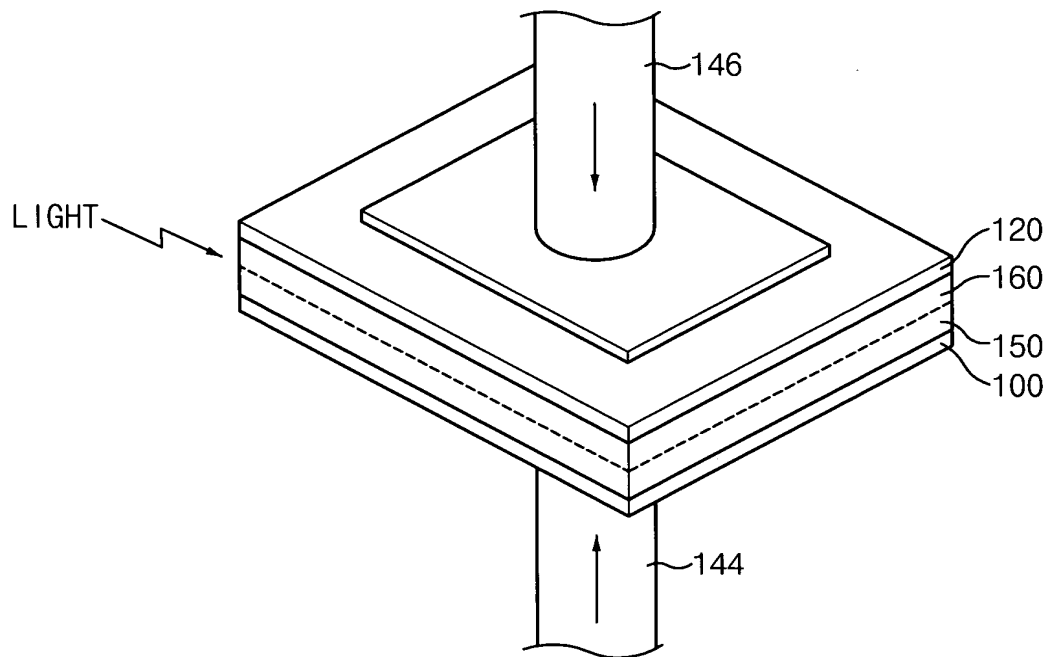


FIG. 8

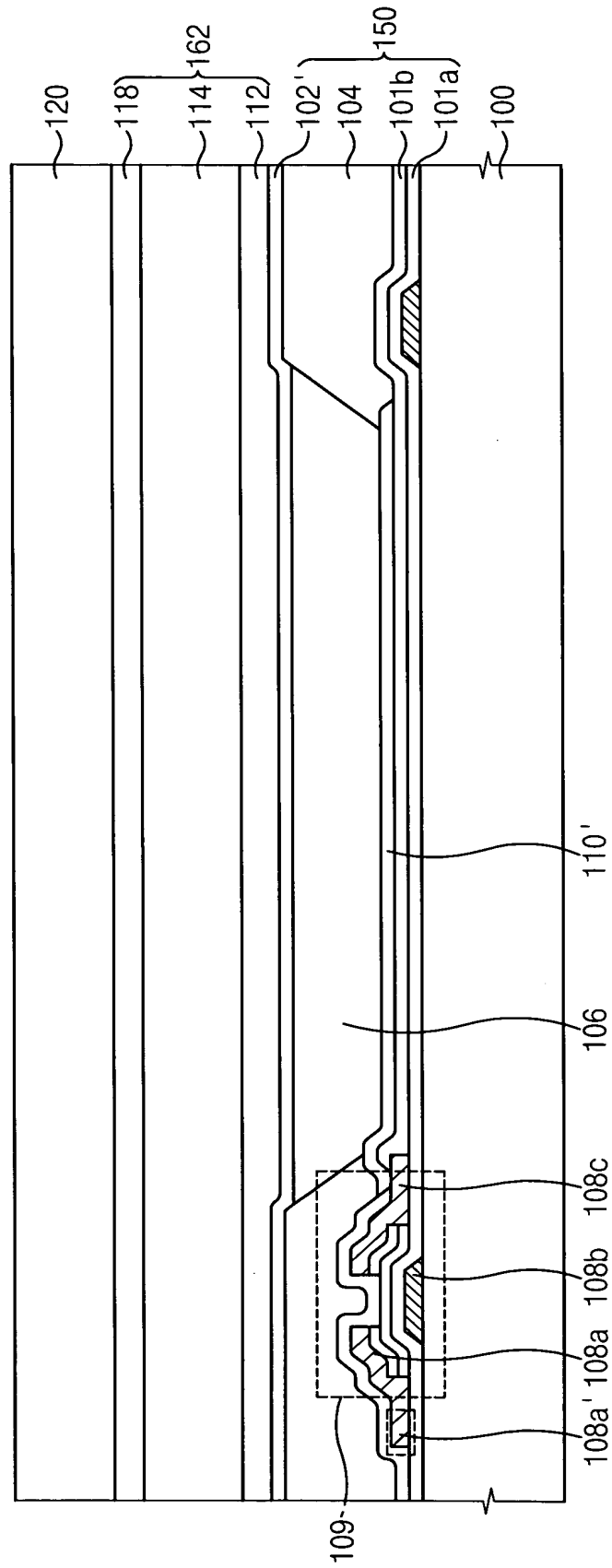




FIG. 9

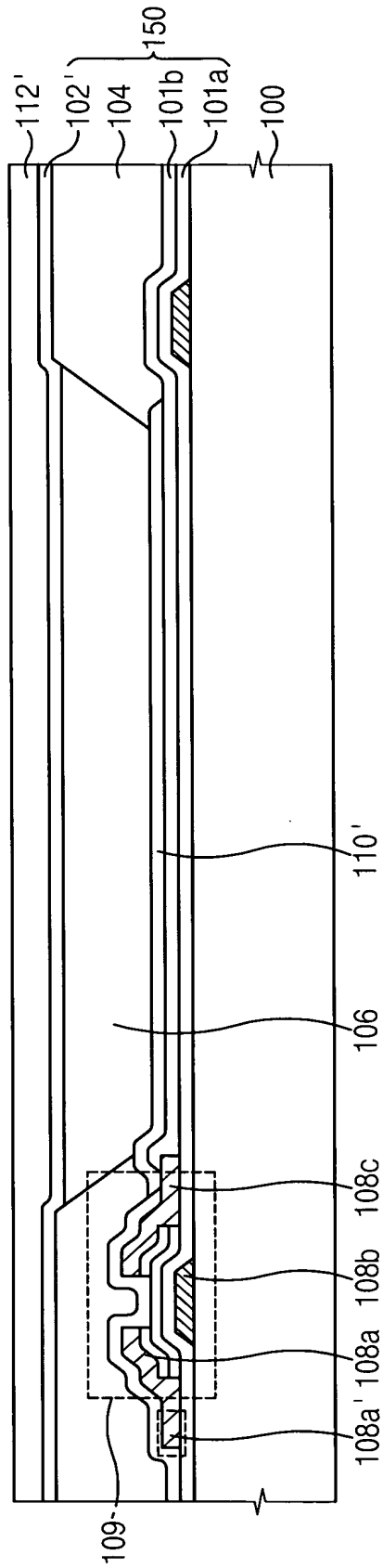


FIG. 10

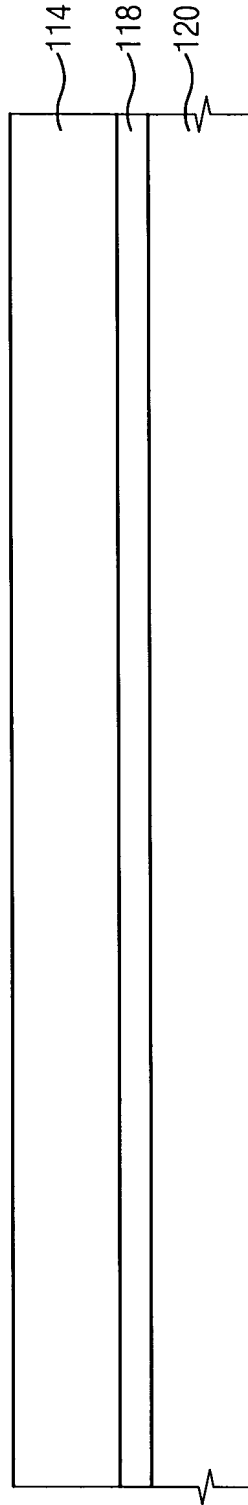


FIG. 11

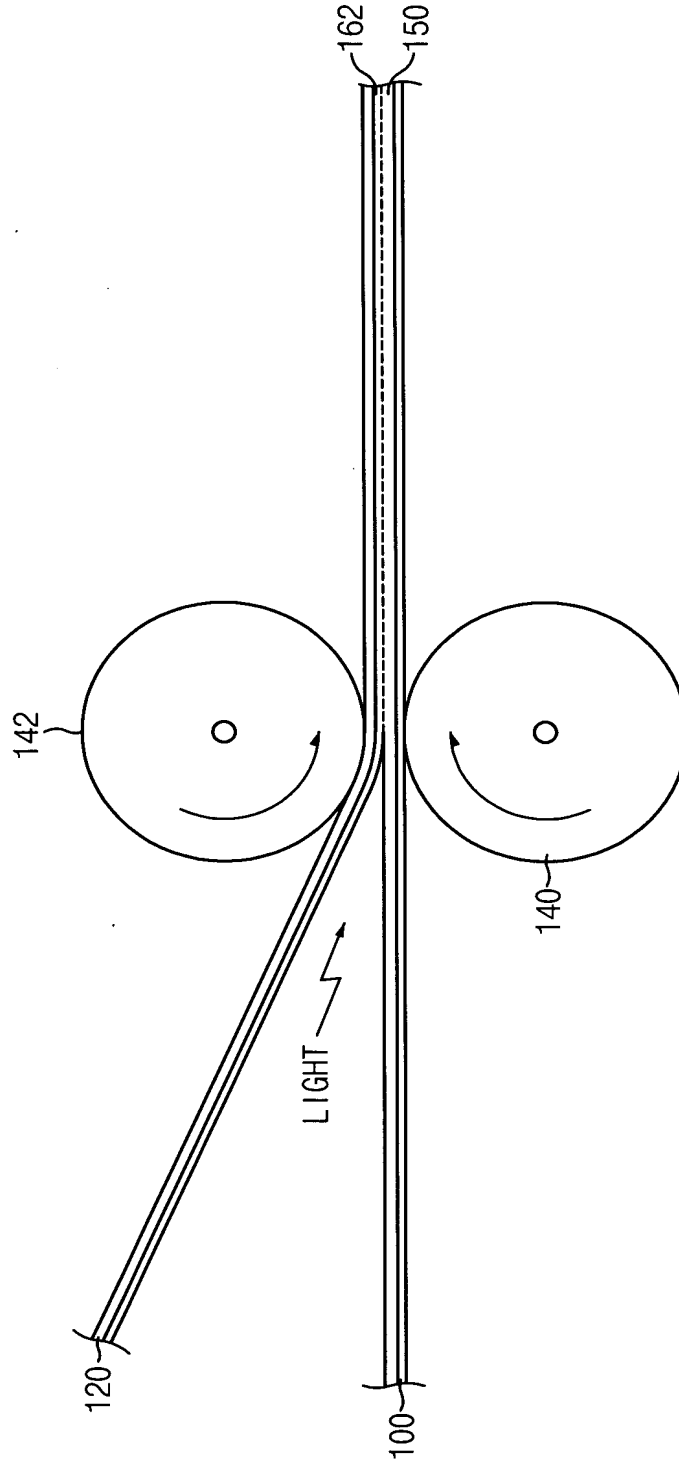


FIG. 12

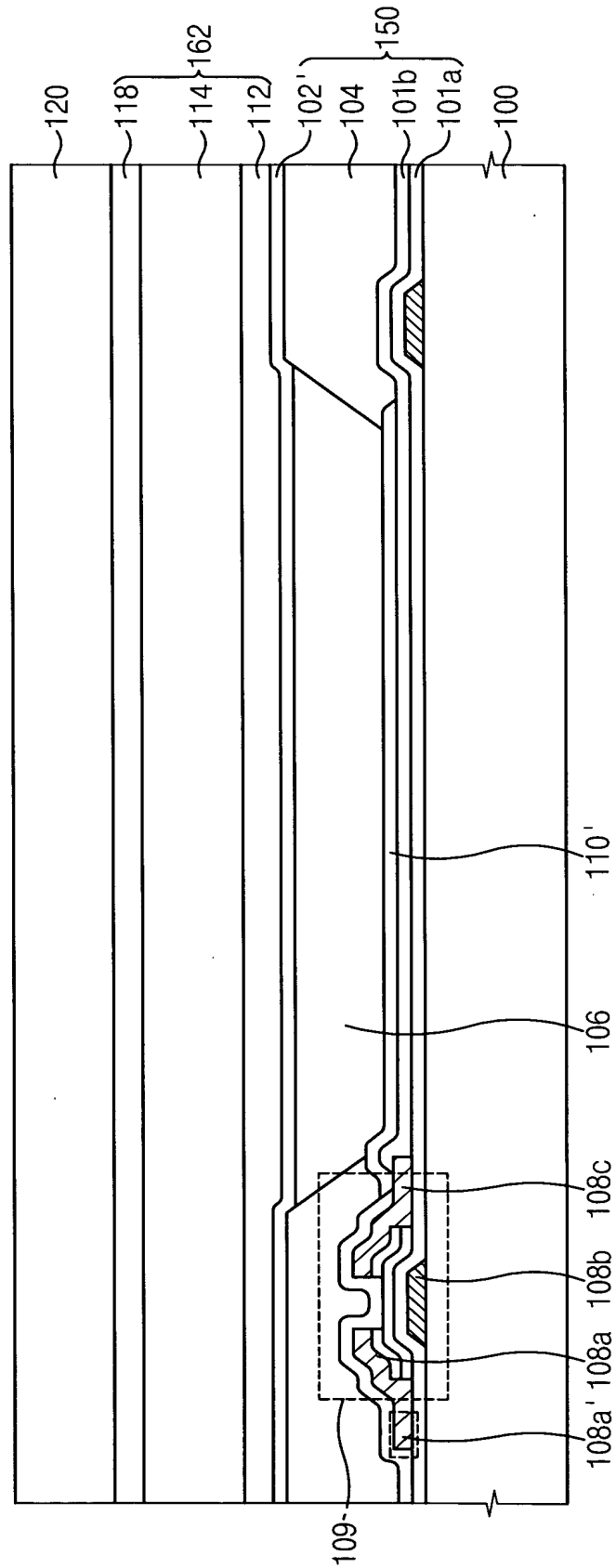




FIG. 14

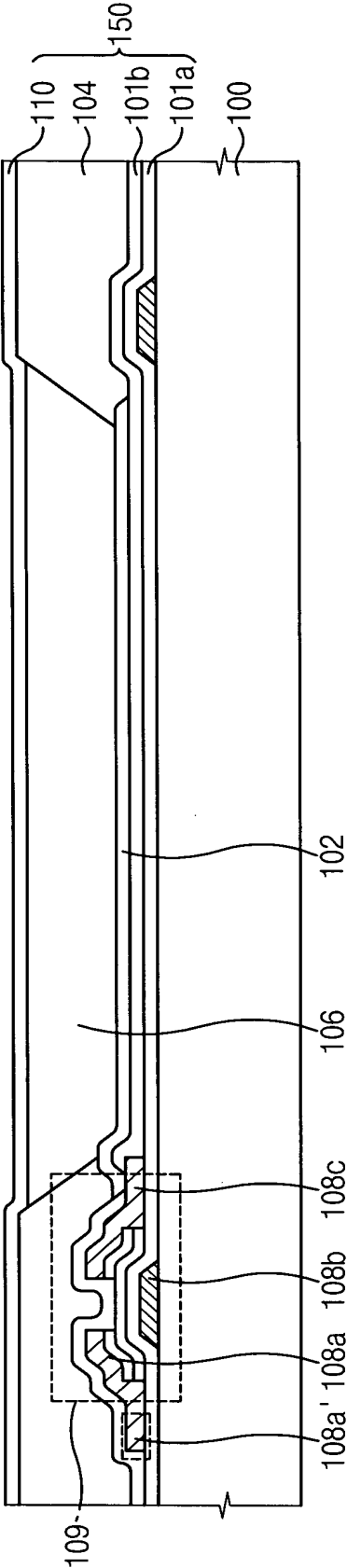


FIG. 15

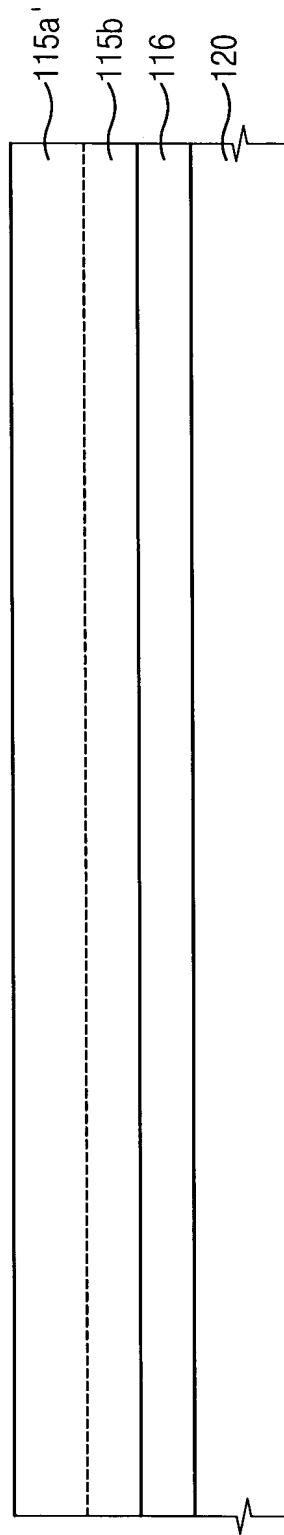


FIG. 16

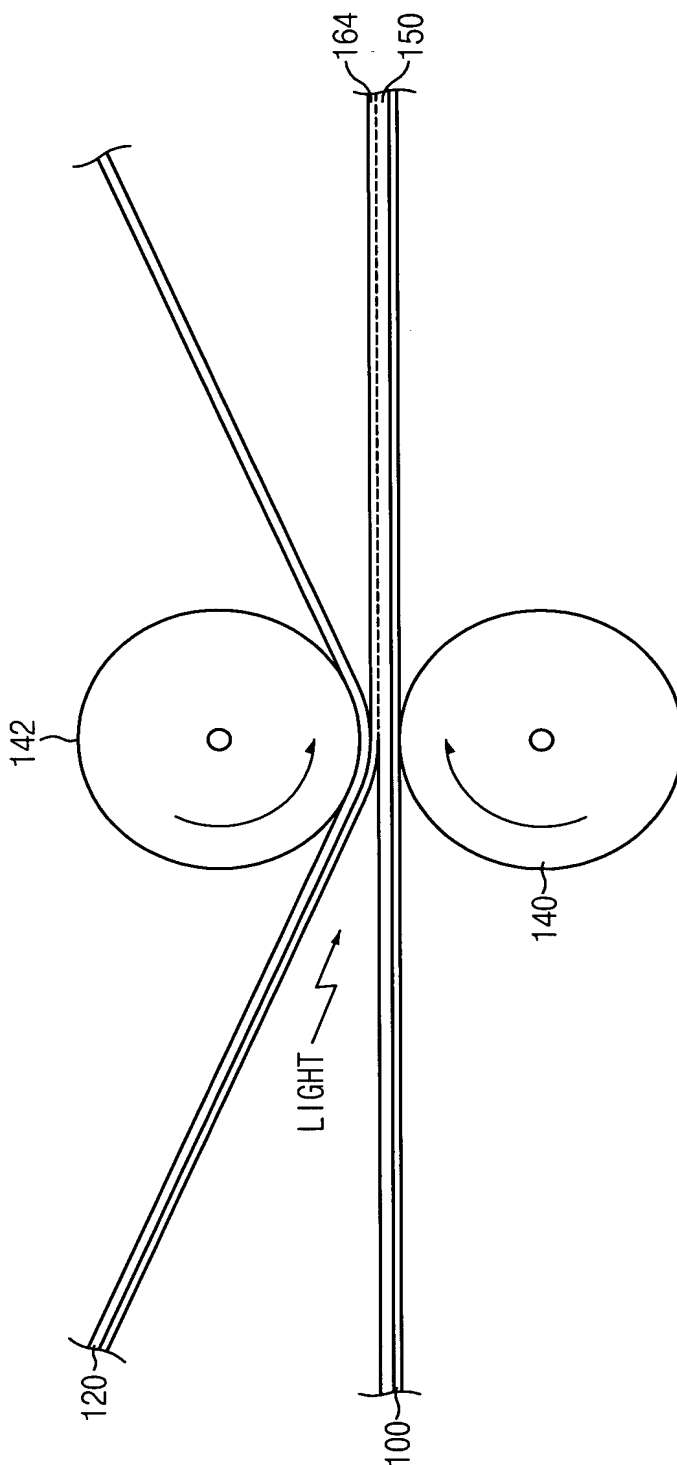




FIG. 17

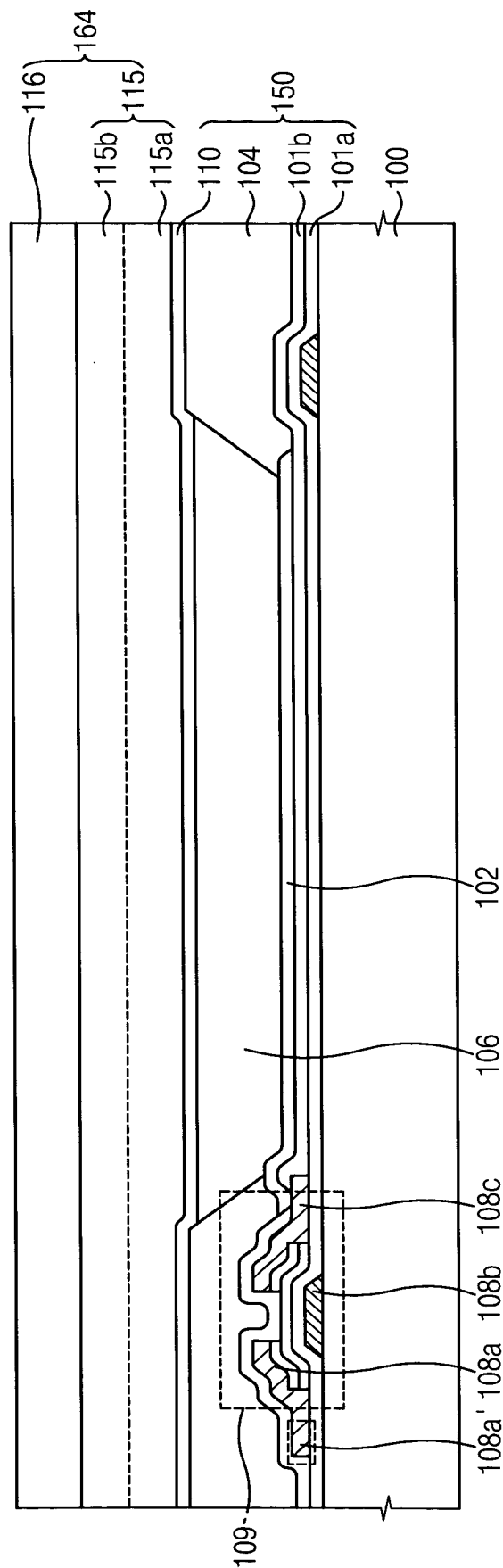


FIG. 18

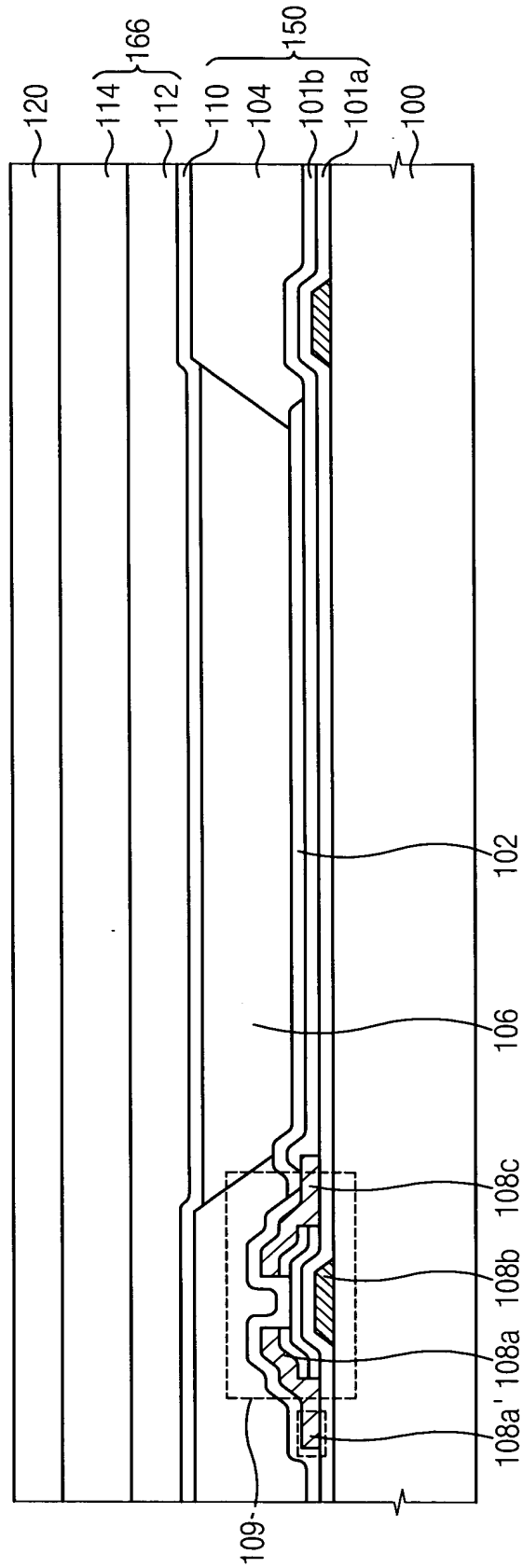


FIG. 19

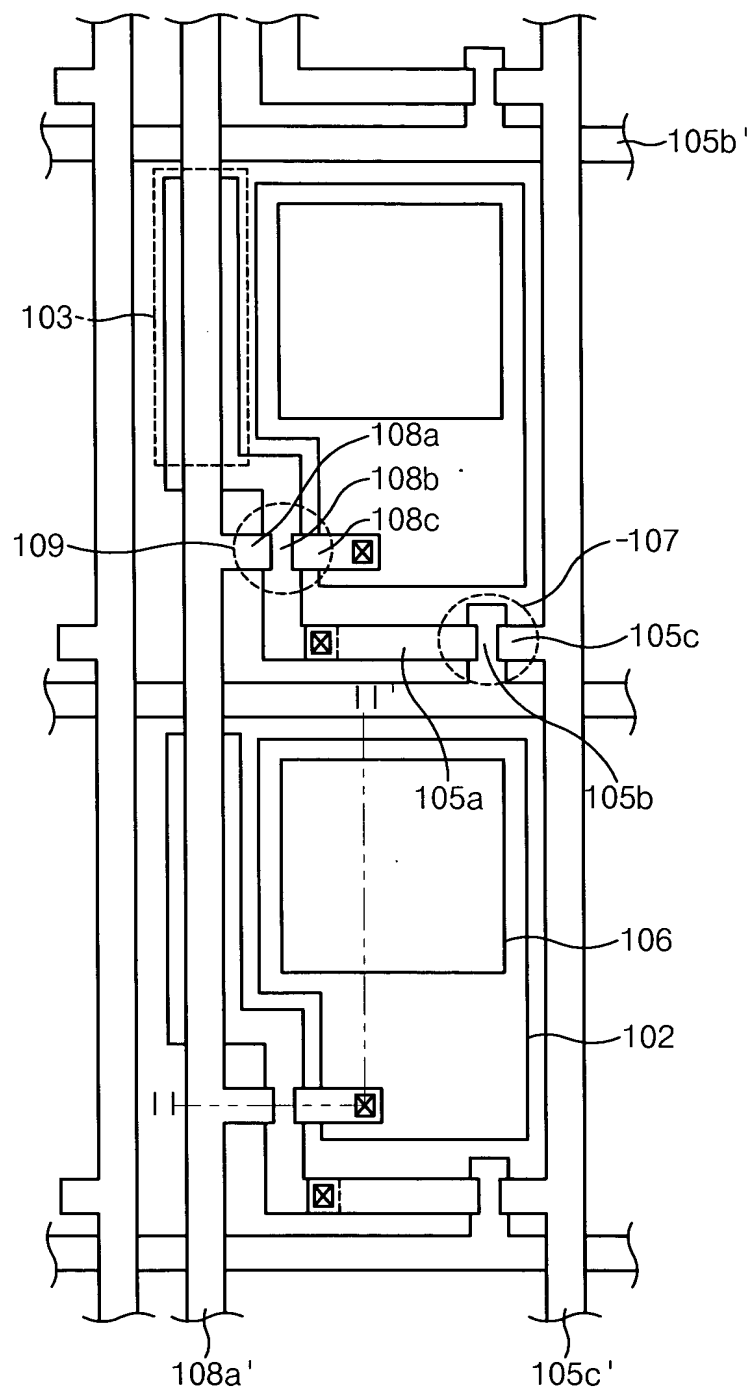


FIG. 20

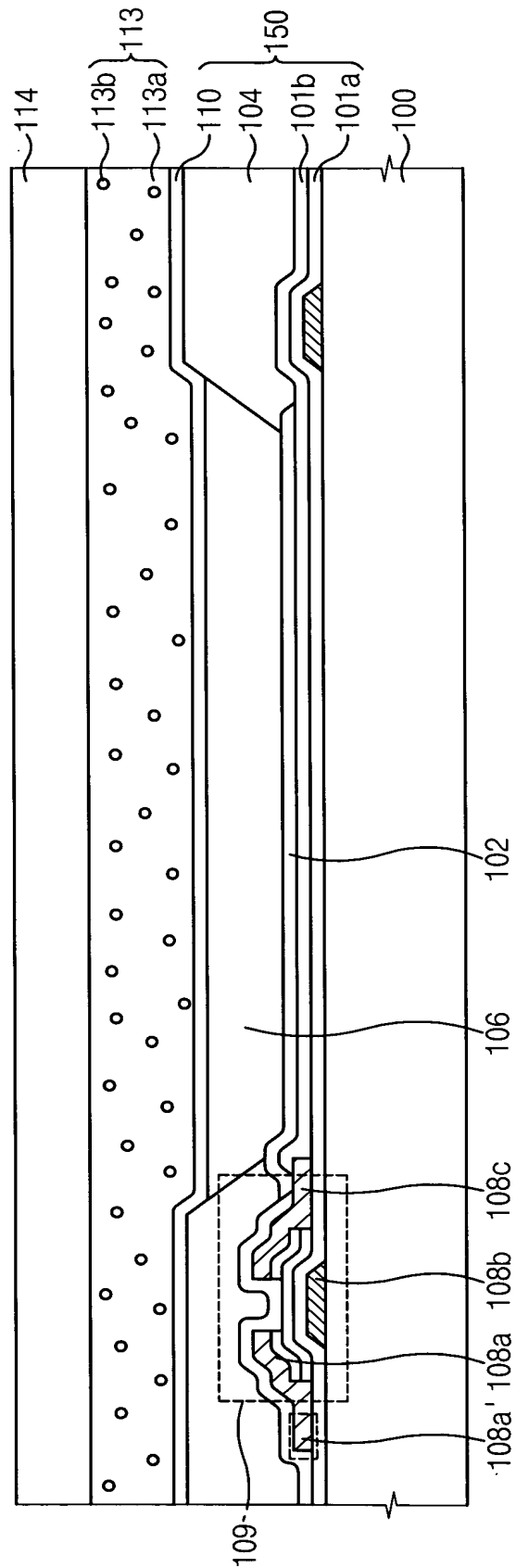


FIG. 21

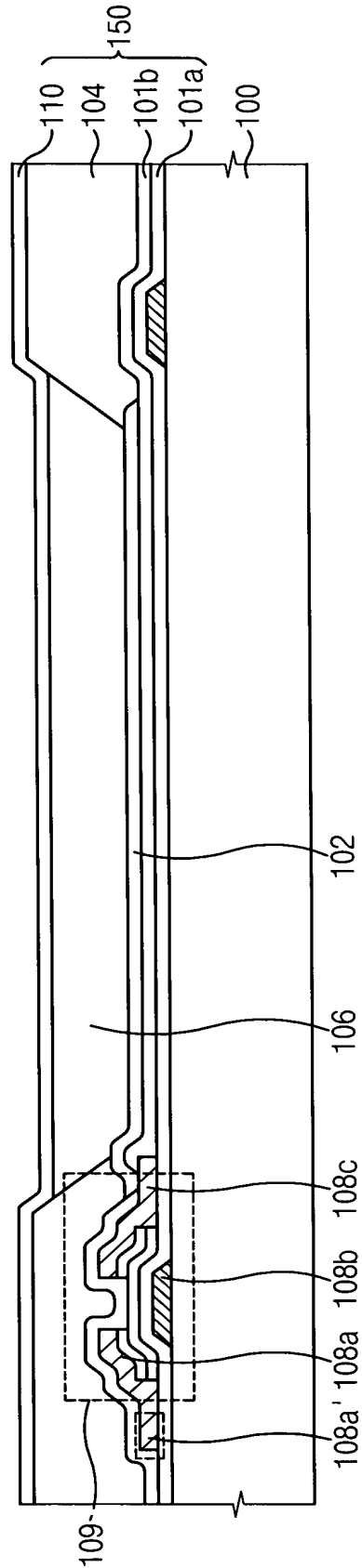


FIG. 22

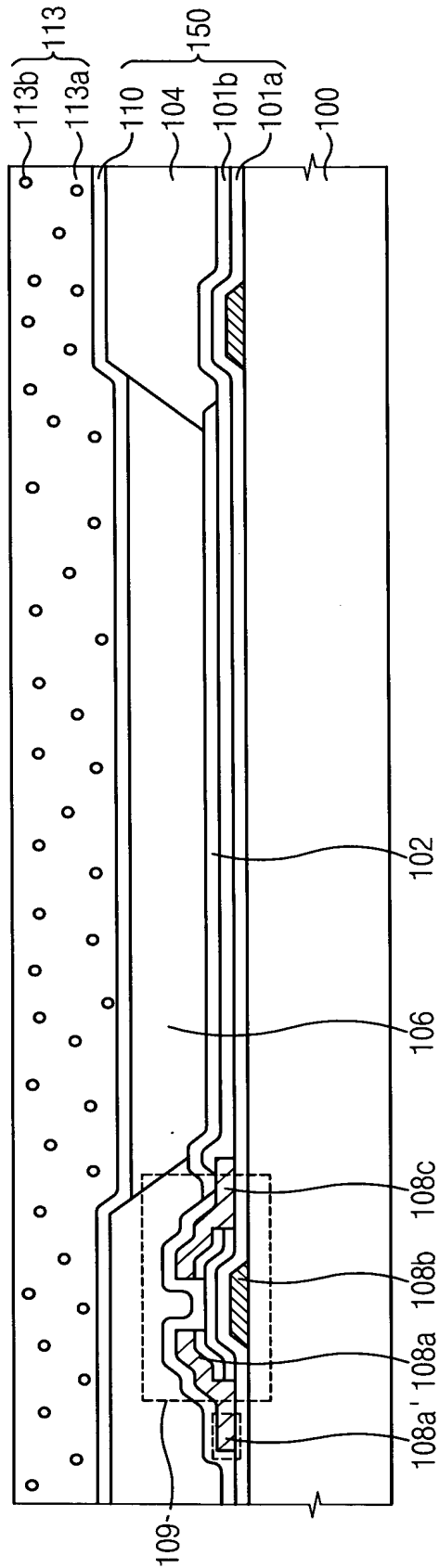


FIG. 23

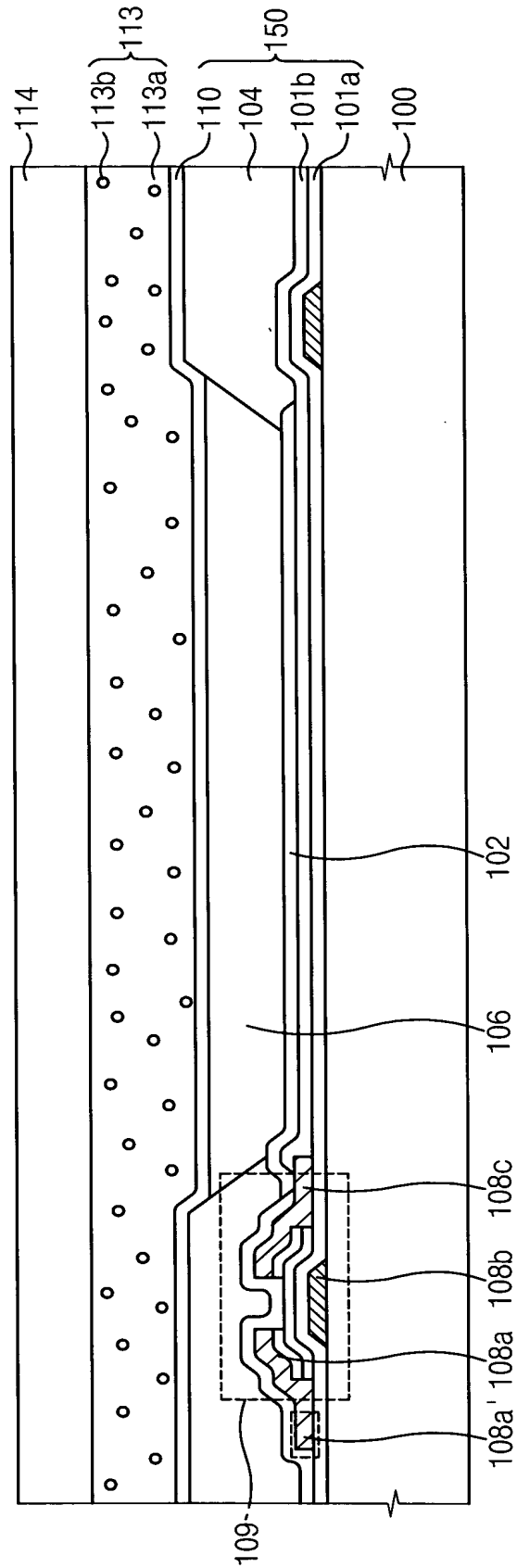


FIG. 24

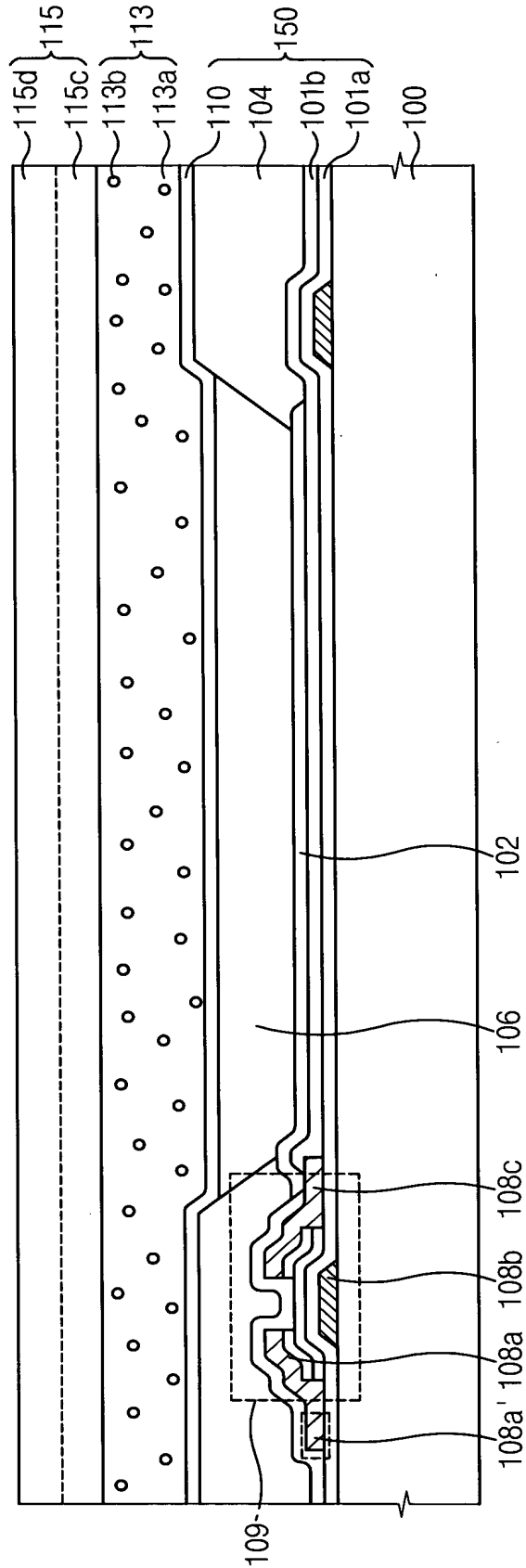




FIG. 25

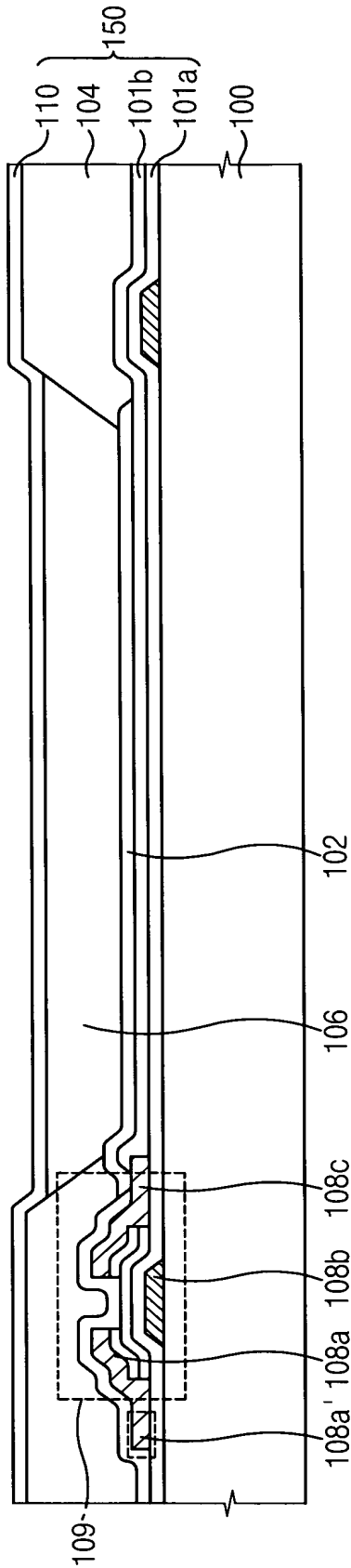


FIG. 26

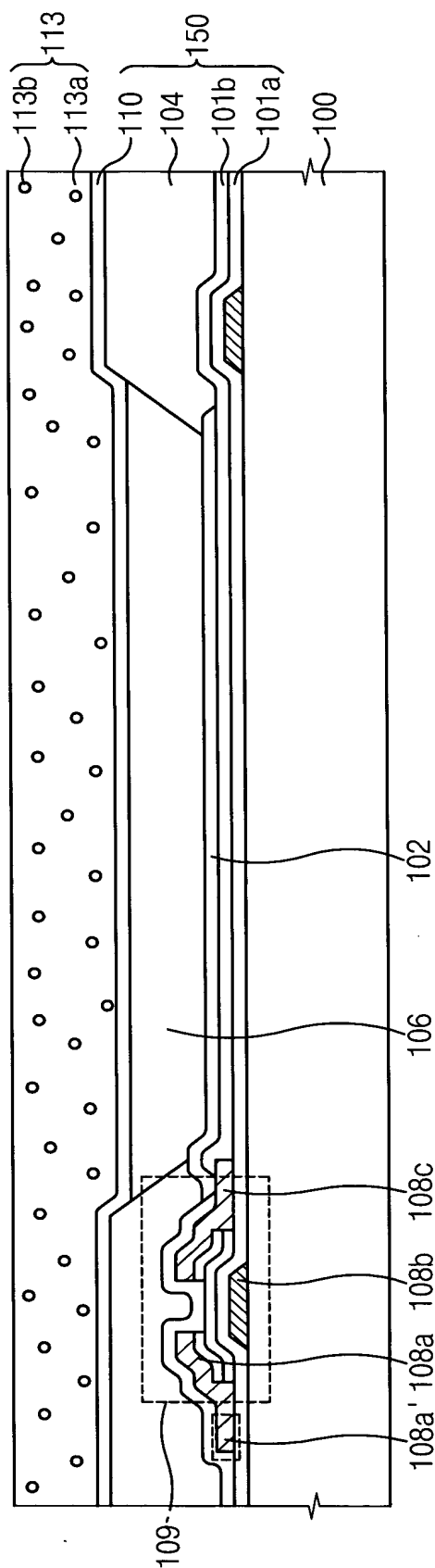


FIG. 27

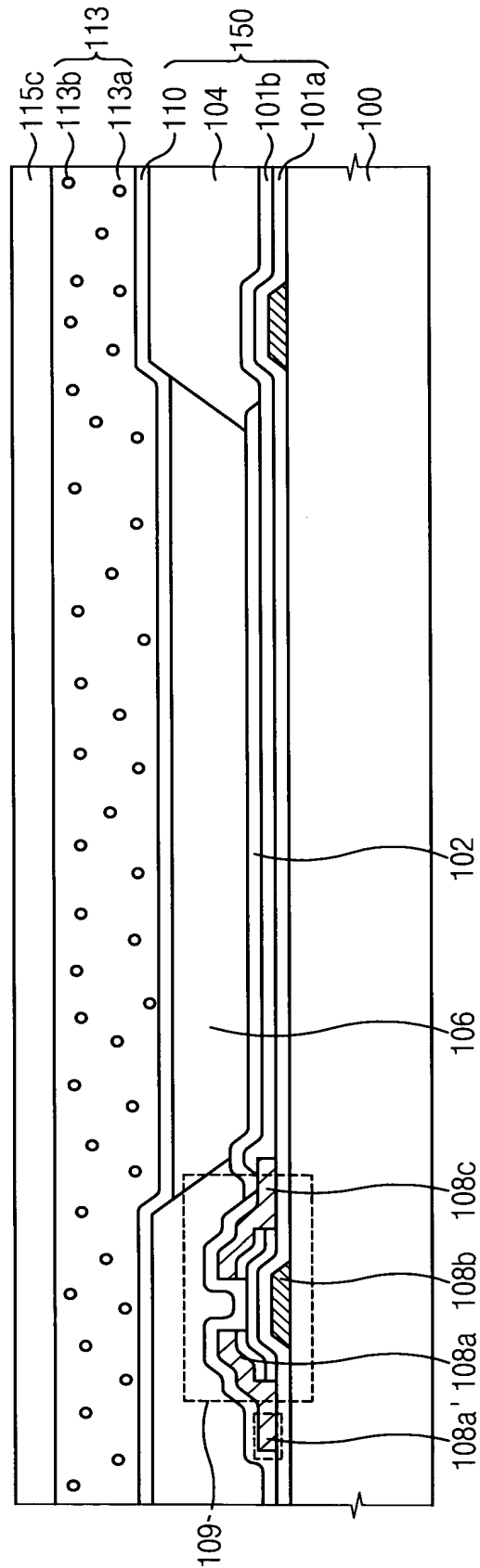
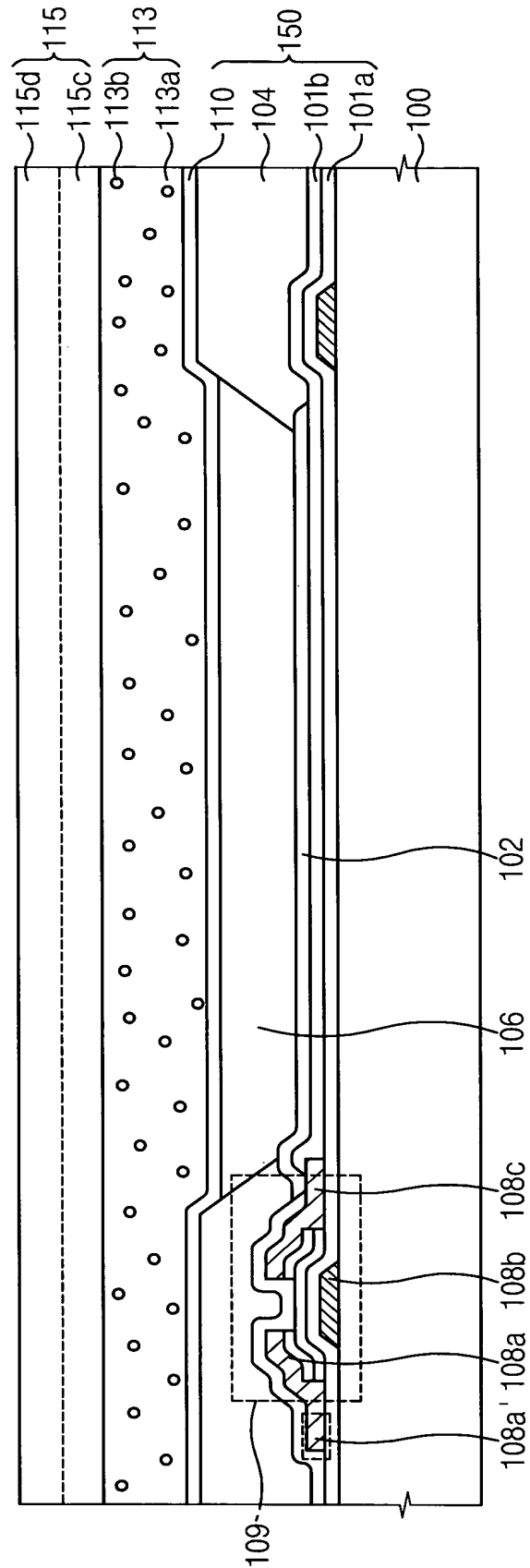


FIG. 28



This cross-sectional view shows a semiconductor device. On the left, a porous layer 100 contains a first conductive layer 101a and a second conductive layer 101b. A third conductive layer 104 is positioned above the porous layer. A layer 110 is located between the porous layer and a substrate 102. The substrate 102 includes a layer 106 and a region 109. A dashed box 108c highlights a portion of the substrate 102, which includes regions 108a, 108a', 108b, and 108b'. Labels 113a and 113b point to specific features within the porous layer 100.

FIG. 30

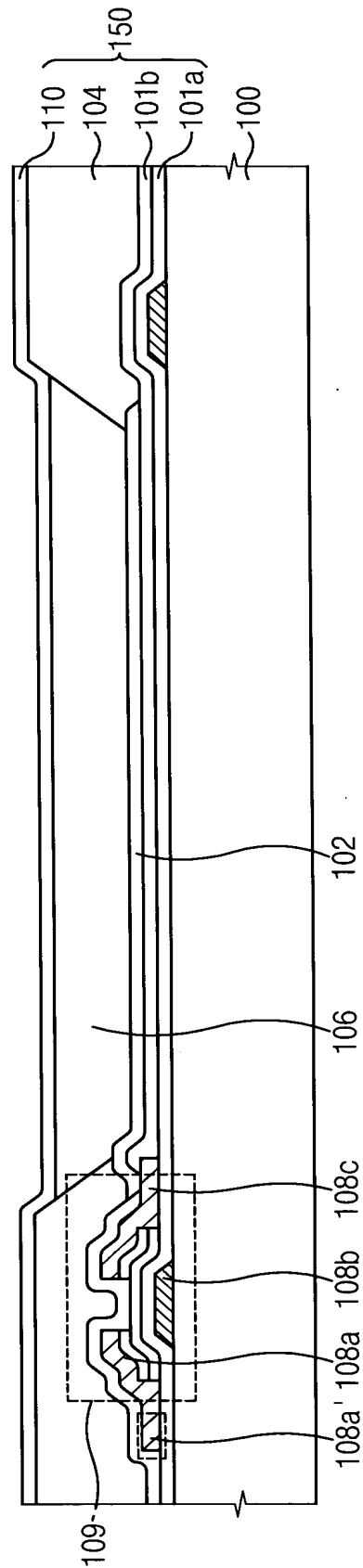


FIG. 31

